

In the Claims

Claims 1-10 (canceled)

Claim 11 (previously presented): A semiconductor processing method comprising:

a masking step providing a common mask; and

an implant step carried out through the common mask, comprising conducting a halo implant of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to at least three of the devices three different respective threshold voltages, wherein the common masking step comprises masking only portions of some of the devices which receive the halo implant, said portions comprising portions of peripheral circuitry devices.

Claim 12 (previously presented): A semiconductor processing method comprising:

a masking step providing a common mask; and

an implant step carried out through the common mask, comprising conducting a halo implant of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to at least three of the devices three different respective threshold voltages, wherein the common masking step comprises masking only portions of some of the devices which receive the halo implant; said devices which receive the halo implant comprise NMOS field effect transistors; and said portions comprise portions of peripheral circuitry devices.

Claim 13 (canceled).

Claim 14 (previously presented): A semiconductor processing method comprising:

a masking step providing a common mask; and

an implant step carried out through the common mask, comprising conducting a halo implant of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to at least three of the devices three different respective threshold voltages, wherein the common masking step comprises masking only portions of some of the devices which receive the halo implant; said devices which receive the halo implant comprise PMOS field effect transistors; and said portions comprise portions of peripheral circuitry devices.

Claim 15 -60 (canceled)